VCO, the VCO constructed as a sequential delay stage and developing multi-phase output signals, each oscillating at the characteristic frequency of the VCO, and each having a phase relationship characterized by an inherent delay of each delay stage;

first frequency divider circuitry disposed between the timing reference signal generator and the comparison circuit, the first frequency divider circuitry dividing the output signal of the timing reference signal generator by a scale factor (NxM) to develop said frequency characteristic provided to said comparison circuit;

second frequency divider circuitry disposed between the timing reference signal generator and an output, wherein the first and second frequency divider circuitry having different frequency division characteristics, the second frequency divider circuitry dividing the output signal of the timing reference signal generator by a scale factor M to develop said desired output clock signal; and

a phase select MUX, the phase select MUX selecting between and among the multi-phase signals to define a respective one as an output clock signal, the phase select MUX being a Gray code MUX, the MUX selecting between and among multi-phase signals in accordance with a phase control word, the phase control word changing states in accordance with a Gray code sequence for reducing jitter when the phase control word change states.

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22. (Unchanged) The timing circuit according to claim 21, wherein the phase control word has a characteristic width J, where J is mathematically dependent on the frequency scale factor M.

REMARKS

The above identified patent application has been amended and reconsideration and reexamination are hereby requested.

The Examiner has rejected Claims 1 - 7 and 12 - 20 under 35 U.S.C. §103 as being unpatentable over Ghoshal in view of Hsu. The Examiner has also rejected Claims 8 - 11 and 21 - 22 under 35 U.S.C. §103 as being unpatentable over Ghoshal in view of Hsu and Barrett et al.

However, Applicants submit that the invention as claimed in amended Claims 8 and 21 is neither taught, described or suggested in Ghoshal even in view of Hsu and Barrett et al.

Applicants' amended Claim 8 calls for (underlining added for emphasis) A <u>phase lock loop</u> comprising ... a timing reference signal generator, connected in feedback fashion to provide a timing reference signal to the detector, the timing reference signal generator being operatively configured to produce an output signal at a characteristic frequency an integral multiple of a desired output clock frequency and to produce an output signal at a characteristic frequency M times the frequency of a desired output clock frequency and being constructed to output <u>multi-phase signals</u>, each phase signal oscillating at the characteristic frequency, wherein the number of phases represented by the multi-phase output signals are reduced by a scale factor M from a number of phases produced by a timing reference signal generator operating at a characteristic frequency substantially equal to a desired output clock frequency ... and ... a <u>phase select MUX</u>, the <u>phase select MUX selecting between and among the multi-phase signals</u> to define a respective one as an output clock signal, <u>the phase select MUX being a Gray code MUX</u>, the MUX selecting between and among multi-phase signals in accordance with <u>a phase control word</u>, the <u>phase control word changing states</u> in accordance <u>with a Gray code sequence for reducing jitter when the phase control word change states</u>.

The present invention provides a phase lock loop configured to reduce jitter. The Gray code mux was chosen to be used in accordance with the present invention because it is an optimal mux for reducing jitter.

With Gray code coding, where only one bit flips at a time when stepping through the Gray code sequence, jitter which would occur when multiple bits are toggling at the same time such as when a binary three is transitioned to a binary four, would be minimized. Further, in accordance with the present invention there is no need to have a mux for a faster control path as suggested by the Examiner.

With Ghoshal teaching a phase lock loop, Hsu teaching a frequency divider circuit for reducing output frequency, and Barrett, while providing for a N stage tree-type MUX, the Applicants submit that there is no suggestion to combine the references, and in particular, to use the teachings of Barrett et al. to use a Gray Code mux in the phase lock loop to reduce jitter as claimed in accordance with the present invention. In particular, there is no suggestion to combine the references to provide a MUX selecting between and among multi-phase signals in accordance with a phase control word, the phase control word changing states in accordance with a Gray code sequence for reducing glitching (i.e., providing low jitter) when the phase control word change states. Barrett is merely attempting to perform a digital decode in an optimal decode sequence.

Accordingly, the Applicants submit that Claim 8 is not unpatentable over Ghoshal in view of Hsu and Barrett et al.

Applicants' amended Claim 21 calls for (underlining added for emphasis) ... A feedback controlled timing circuit, comprising: ... a timing reference signal generator, ... the timing reference signal generator being implemented as a VCO, the VCO constructed as

a sequential delay stage and developing multi-phase output signals, each oscillating at the characteristic frequency of the VCO, and each having a phase relationship characterized by an inherent delay of each delay stage ... and ... a phase select MUX, the phase select MUX selecting between and among the multi-phase signals to define a respective one as an output clock signal, the phase select MUX being a Gray code MUX, the MUX selecting between and among multi-phase signals in accordance with a phase control word, the phase control word changing states in accordance with a Gray code sequence for reducing jitter when the phase control word change states.

Therefore, the Applicants submit that Claim 21 is not unpatentable over Ghoshal in view of Hsu and Barrett et al. for the same reasons set forth above for Claim 8.

Claims 3, 9 - 11 are dependent on Claim 8. Claims 19 and 22 are dependent on Claim 21. As such these dependent claims are believed allowable based upon Claims 8 and 21 respectively.

Accordingly, in view of the above amendment and remarks it is submitted that the claims are patentably distinct over the prior art and that all the rejections to the claims have been overcome. Reconsideration and reexamination of the above Application is requested.

Attached hereto is a marked-up version of the changes made to the specification and claims by the current amendment. Unchanged claims have been included for the Examiner's reference convenience. The

attached page is captioned "**<u>Version with markings to show changes made</u>**."

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE
(UNCHANGED CLAIMS ARE INCLUDED FOR REFERENCE PURPOSES)

3. (Amended) The phase lock loop according to claim 8 [2], further comprising a loop filter coupled between the phase/frequency detector and the timing reference generator, the loop filter developing a control voltage for the timing reference generator.

8. (Amended) A phase lock loop comprising:

a detector for comparing a phase or frequency characteristic of an input signal to a phase or frequency characteristic of a timing reference signal;

a timing reference signal generator, connected in feedback fashion to provide a timing reference signal to the detector, the timing reference signal generator being operatively configured to produce an output signal at a characteristic frequency an integral multiple of a desired output clock frequency and to produce an output signal at a characteristic frequency M times the frequency of a desired output clock frequency and being constructed to output multi-phase signals, each phase signal oscillating at the characteristic frequency, wherein the number of phases represented by the multi-phase output signals are reduced by a scale factor M from a number of phases produced by a timing reference signal generator operating at a characteristic frequency substantially equal to a desired output clock frequency;

a frequency divider circuit coupled to receive the output signal and reduce its characteristic frequency to a desired output clock frequency; and

a phase select MUX, the phase select MUX selecting between and among the multi-phase signals to define a respective one as an output clock signal, [The phase lock loop according to

claim 7, wherein] the phase select MUX being [is] a Gray code MUX, the MUX selecting between and among multi-phase signals in accordance with a phase control word, the phase control word changing states in accordance with a Gray code sequence for reducing jitter when the phase control word change states.

9. (Unchanged) The phase lock loop according to claim 8, wherein the phase control word has a characteristic width J, where J is mathematically dependent on the frequency scale factor M.

10. (Unchanged) The phase lock loop according to claim 9, wherein the frequency divider circuit is constructed of current mode logic components.

11. (Unchanged) The phase lock loop according to claim 9, wherein the phase control MUX is constructed of current mode logic components.

19. (Amended) The timing circuit according to claim 21 [18], wherein the number of phases represented by the multi-phase output signals are reduced by a scale factor M from a number of phases produced by a timing reference signal generator operating at a characteristic frequency substantially equal to a desired output clock frequency.

21. (Amended) A feedback controlled timing circuit, comprising:

a comparison circuit configured to compare a frequency characteristic of an input signal to a frequency characteristic of a timing reference signal, the comparison circuit asserting control signals in response to said comparison;

a timing reference signal generator, connected to provide a timing reference signal to the comparison circuit, the timing reference signal generator responsive, in feedback fashion, to said control signals asserted by the comparison circuit, the timing reference signal generator being configured to develop an output signal at a frequency M times the frequency of a desired output clock signal, the desired output clock signal having a frequency characteristic N times the frequency characteristic of the input signal, the timing reference signal generator being implemented as a VCO, the VCO constructed as a sequential delay stage and developing multi-phase output signals, each oscillating at the characteristic frequency of the VCO, and each having a phase relationship characterized by an inherent delay of each delay stage;

first frequency divider circuitry disposed between the timing reference signal generator and the comparison circuit, the first frequency divider circuitry dividing the output signal of the timing reference signal generator by a scale factor (NxM) to develop said frequency characteristic provided to said comparison circuit;

second frequency divider circuitry disposed between the timing reference signal generator and an output, wherein the first and second frequency divider circuitry having different frequency division characteristics, the second frequency divider circuitry dividing the output signal of the timing reference signal generator by a scale factor M to develop said desired output clock signal; and

a phase select MUX, the phase select MUX selecting between and among the multi-phase signals to define a respective one as an output clock signal, [The timing circuit according to claim 20, wherein] the phase select MUX being [is] a Gray code MUX, the MUX selecting between and among multi-phase signals in accordance with

a phase control word, the phase control word changing states in accordance with a Gray code sequence for reducing jitter when the phase control word change states.

22. (Unchanged) The timing circuit according to claim 21, wherein the phase control word has a characteristic width J, where J is mathematically dependent on the frequency scale factor M.

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